

<PRESS RELEASE>

To whom it may concern:



November 13, 2025

TAIYO HOLDINGS CO. LTD.

Next-generation Semiconductor-packaging Material “FPIM™ Series” It’s First Successful Formation of 3-layer RDL with CD 1.6 μm on 12-inch Wafer

-Paper Presented at the 14th IEEE CPMT Symposium Japan (ICSJ 2025)

On November 13, 2025, Taiyo Holdings Co., Ltd. (Securities Code: 4626; hereinafter referred to as "Taiyo Holdings"), based in Tokyo, presented a paper, co-authored with imec, one of the world's largest semiconductor research institutions, at the 14th IEEE CPMT Symposium Japan (ICSJ2025), focusing on the “FPIM™ Series” (hereinafter referred to as “this material”), a negative-type photosensitive insulating material for fine-pitch RDLs^{*1} designed for the damascene process, developed as a next-generation semiconductor packaging material, with imec, one of the world's largest semiconductor research institutions, at the 14th IEEE CPMT Symposium Japan (ICSJ2025).

RDL is an important technology in the most advanced structures of semiconductor packaging for more efficient electrical connections, and it is currently manufactured mainly by the semi-additive process (SAP)^{*2}. imec proposes that, in the future, as finer wiring is pursued, the damascene process^{*3} will become essential for forming interconnects with a line spacing of 1.6 μm or less. In response, Taiyo Holdings has been developing this material as a next-generation fine-pitch RDL material for the damascene process and has been conducting joint research with imec since October 2022. In this study, a three-layer RDL structure was formed on a 12-inch wafer using this material, and evaluations were carried out. Each wiring pitch achieved the target dimensions as follows: CD^{*4} 1.6 μm for the RDL1 layer on the wafer, CD 2.0 μm (with a via center-to-center pitch of CD 4.0 μm) for the via layer, and CD 1.6 μm for the RDL2 layer. These values are extremely close to the resolution limit of the low NA stepper^{*5} used in this study. In addition, the evaluation results of the electrical characteristics, specifically, leakage current and resistance, of the RDL1 layer with CD 1.6 μm were favorable. As an outcome of this joint research with imec, it was confirmed that this material possesses excellent electrical properties, high resolution, and quality suitable for adaptation to the CMP process^{*6}.

In the future, the company aims to achieve the formation of RDLs on wafers with a wiring pitch of CD 500 nm or less, while continuing to verify the long-term performance of electrical characteristics and reliability. Taiyo Holdings will continue developing materials that contribute to advances in the semiconductor packaging field, including further performance enhancement of AI semiconductors. In addition, shipment of small-quantity samples of this material for R&D purposes began in 2025.

^{*1} RDL (redistribution layer) is a layer formed on the surface of a semiconductor chip to redistribute electrical wiring.

^{*2} A method in which a thin seed layer is first formed over the entire surface, and then wiring patterns are formed by electroplating on the wiring areas.

^{*3} A method in which grooves for wiring are formed on an insulating film, and the grooves are filled and patterned using sputtering, CVD, electroplating, or similar processes.

^{*4} CD (critical dimension) refers to the dimensions of fine patterns.

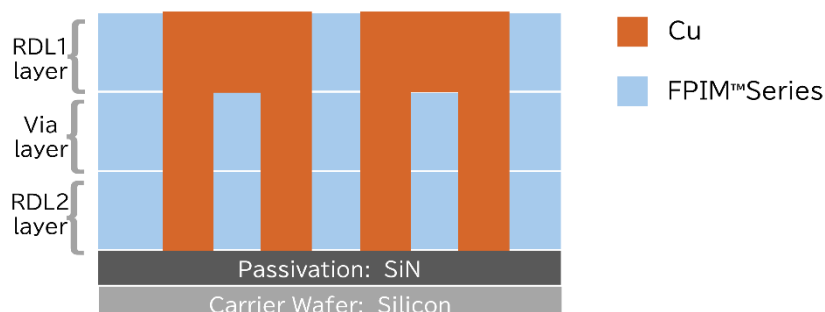
^{*5} Veeco Low NA (0.16) i-line exposure system AP300 (first generation).

^{*6} CMP process (chemical mechanical planarization/polishing) is a process in semiconductor manufacturing that chemically and mechanically planarizes the wafer surface.

<PRESS RELEASE>

[Title of co-authored paper] Development of 1.6 μm Fine-Pitch RDL Damascene Process using Low-NA i-Line Stepper and a New Negative-tone Photosensitive Dielectric Material

[Structure of evaluation sample]



[Product image]



■ About the Collaboration Between imec and Taiyo Holdings

imec, which is short for “Interuniversity Microelectronics Centre,” is one of the world’s largest semiconductor research institutes, headquartered in Belgium. It promotes open innovation by collaborating with universities and companies around the world, contributing to the development of cutting-edge semiconductor technologies. In October 2022, imec and Taiyo Holdings began joint research on a negative-type photosensitive insulating material for fine-pitch RDLs used in the damascene process—a next-generation semiconductor packaging material. Since November 2024, Taiyo Holdings has dispatched resident researchers to imec to establish an environment for smoother collaboration and continues daily research and development of advanced semiconductor materials.

[Product inquiries and information requests]

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