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To whom it may concern:

September 10, 2026

TAIYO HOLDINGS CO. LTD.

Taiyo Holdings Launches Next-generation Semiconductor-packaging Material "FPIM Series,"

- Achieving Its First Three-layer RDL Formation with 700-nm CD on 12-inch Wafers

On September 10, 2026, Taiyo Holdings Co., Ltd. (Securities Code: 4626; hereinafter referred to as "Taiyo Holdings"), based in Tokyo, presented a paper, at the 11th IEEE Electronics System-Integration Technology Conference (IEEE ESTC 2026), held in Helsinki, Finland, on the "FPIM Series" (hereinafter the "Material"), a next-generation semiconductor-packaging material. The FPIM Series is a fine-pitch RDL[*1] negative-tone i-line photosensitive insulating material for dual damascene processes.

This paper was co-authored with imec, one of the world's largest semiconductor research institutes. The RDL is a key technology in advanced semiconductor-packaging structures, enabling more efficient electrical connections. Currently, RDLs are manufactured mainly using the semi-additive process (SAP)[*2]. According to imec, as the industry pursues increasingly fine-pitch wiring, the dual damascene process[*3] will become essential for forming wiring with pitches of 1.6 micrometers or less. To address this, Taiyo Holdings developed the Material as a next-generation fine-pitch RDL material for dual damascene processes and began joint research with imec in October 2022. In November 2025, the two organizations presented a co-authored paper on the formation of a three-layer RDL structure with a CD[*4] of 1.6 micrometers on 12-inch wafers.

In this research, a three-layer RDL structure was formed on 12-inch wafers using the Material and evaluated. As a result, the target dimension of 700-nm CD was achieved for both interconnects and vias. The 700-nm CD metal 1 layer (M1) also demonstrated favorable electrical characteristics in terms of leakage current and resistance. Through this joint research with imec, it was confirmed that the Material offers excellent electrical characteristics and high resolution and is suitable for use with the CMP process[*5]. These results represent an important achievement in interconnect technology for next-generation advanced packaging, paving the way for the future development of submicron-class RDL design rules.

Going forward, Taiyo Holdings aims to achieve RDL formation with a CD of 500 nm or less on wafers, while continuing to verify the long-term performance and reliability of the electrical characteristics. The company will continue developing materials that contribute to the growth of the semiconductor packaging field, such as by enabling further improvements in the performance of AI semiconductors. Taiyo Holdings also began shipping small-volume samples of the Material for R&D applications in 2025.

[*1] RDL (redistribution layer) is a layer formed on the surface of a semiconductor chip to redistribute electrical wiring.
[*2] A method in which a thin seed layer is first formed over the entire surface, and then wiring patterns are formed by electroplating on the wiring areas.
[*3] A method in which grooves for wiring are formed on an insulating film, and the grooves are filled and patterned using sputtering, CVD, electroplating, or similar processes.
[*4] CD (critical dimension) refers to the dimensions of fine patterns.
[*5] CMP process (chemical mechanical planarization/polishing) is a process in semiconductor manufacturing that chemically and mechanically planarizes the wafer surface.

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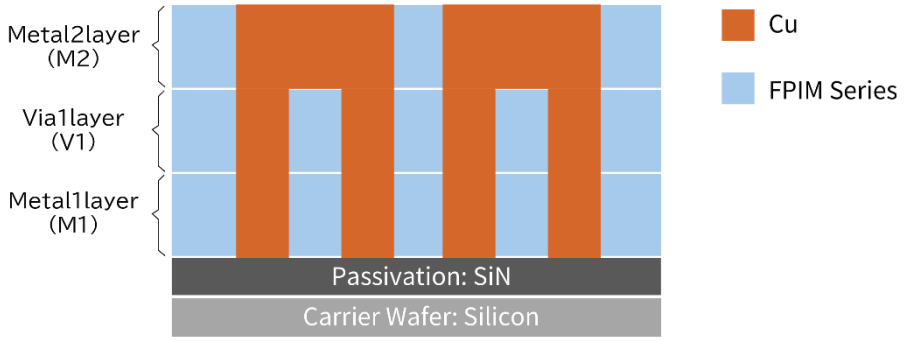
■Conference information & presentation details

Name of conference: The 11th IEEE Electronics System-Integration Technology Conference
Location: Helsinki, Finland
Dates: From Wednesday, September 9, to Friday, September 11, 2026
Presentation session: MIP 1: Dielectric and Glass Materials for Advanced Substrates
Co-authored paper title: A Novel i-Line Photosensitive Dielectric Material Enabling 700 nm Polymer Damascene RDL for Advanced Packaging
Related Link: https://www.estc-conference.net/



<Production of Evaluation Samples>

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■ About the Collaboration Between imec and Taiyo Holdings

Headquartered in Belgium, imec is one of the world's leading research and innovation hubs for advanced semiconductor technology. It promotes open innovation in collaboration with universities and companies around the world, contributing to the development of cutting-edge semiconductor technologies. In October 2022, imec and Taiyo Holdings began joint research on a fine-pitch RDL negative-tone photosensitive insulating material for damascene processes, a material for next-generation semiconductor packaging. Since November 2024, Taiyo Holdings has also dispatched personnel to be stationed at imec to facilitate closer collaboration, while conducting ongoing research and development of advanced semiconductor materials. In November 2025, the two organizations announced that they had achieved a wiring CD of 1.6 micrometers and a via CD of 2 micrometers on 12-inch wafers using the "FPIM Series" RDL material.

[Product inquiries and information requests]
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https://www.taiyo-hd.co.jp/en/contact/contact-rd-en.html